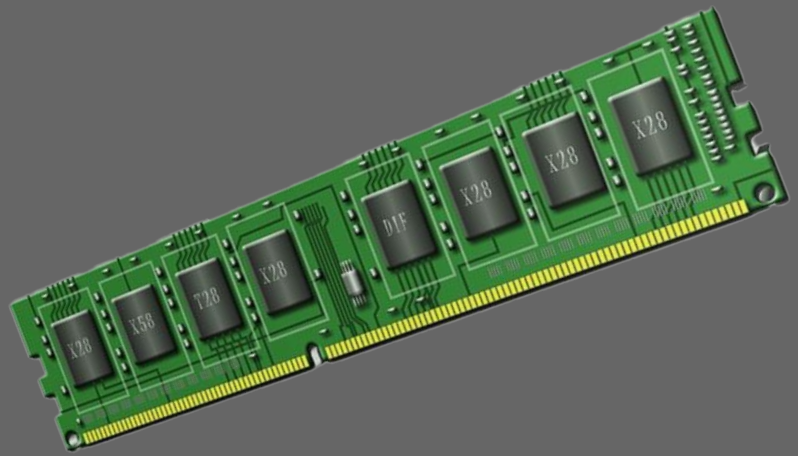
CPE 470 - RAM



Glossary

RAM: Random Access Memory

RAM

- Used to Behavioral RAM in FPGA Land
  - `reg [31:0] ram [1023:0];`
- In ASIC Land, have to use IP

- Tradeoffs between capacity and latency
  - Fast memories ⟶ small
  - Large memories ⟶ slow

- Often Analog
  - Most Memory cells are analog structures
  - Exception: Registers/ Flip Flops

Technologies have vastly different tradeoffs between capacity, access latency, bandwidth, energy, and cost
– … and logically, different applications

	Capacity	Latency	Cost/GB	
Register	1000s of bits	20 ps	$$$$	Processor Datapath
SRAM	~10 KB-10 MB	1-10 ns	~$1000	Memory Hierarchy
DRAM	~10 GB	80 ns	~$10	
Flash*	~100 GB	100 us	~$1	I/O subsystem
Hard disk*	~1 TB	10 ms	~$0.10	

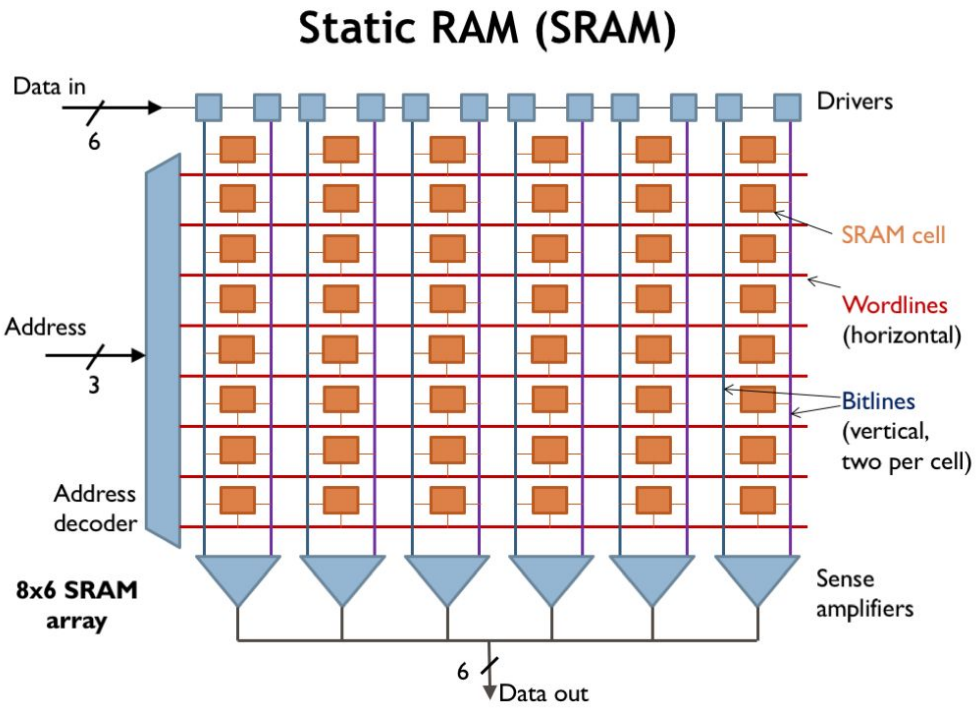
* non-volatile (retains contents when powered off)

Glossary

SRAM: Static RAM

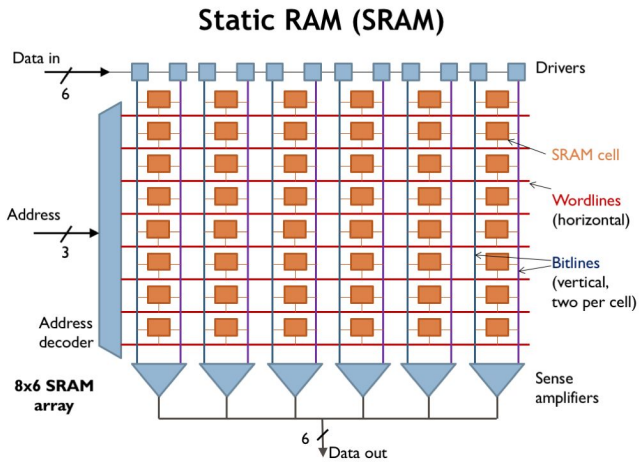
SRAM

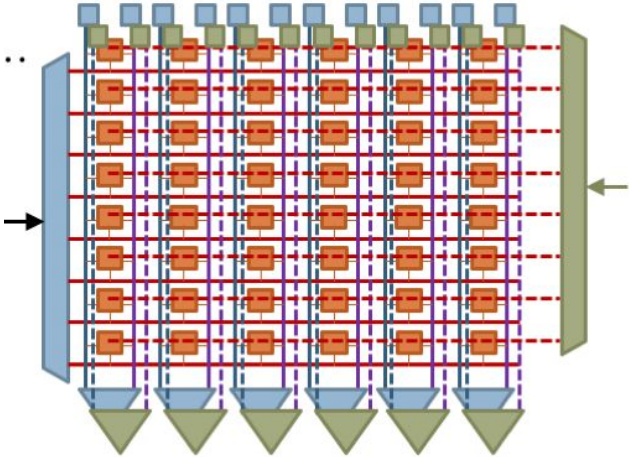
- Fastest On-Chip RAM
  - Except for flip flops which are not RAM
- Volatile Memory
  - Stores data as long as power is supplied
- 6 transistors per bit cell
  - Useful as a metric of size
  - More transistors = less dense
- Analog
  - Requires sense amplifiers to read each bit
  - Must be simulated with behavioral model, not gate-level



SRAM - Ports

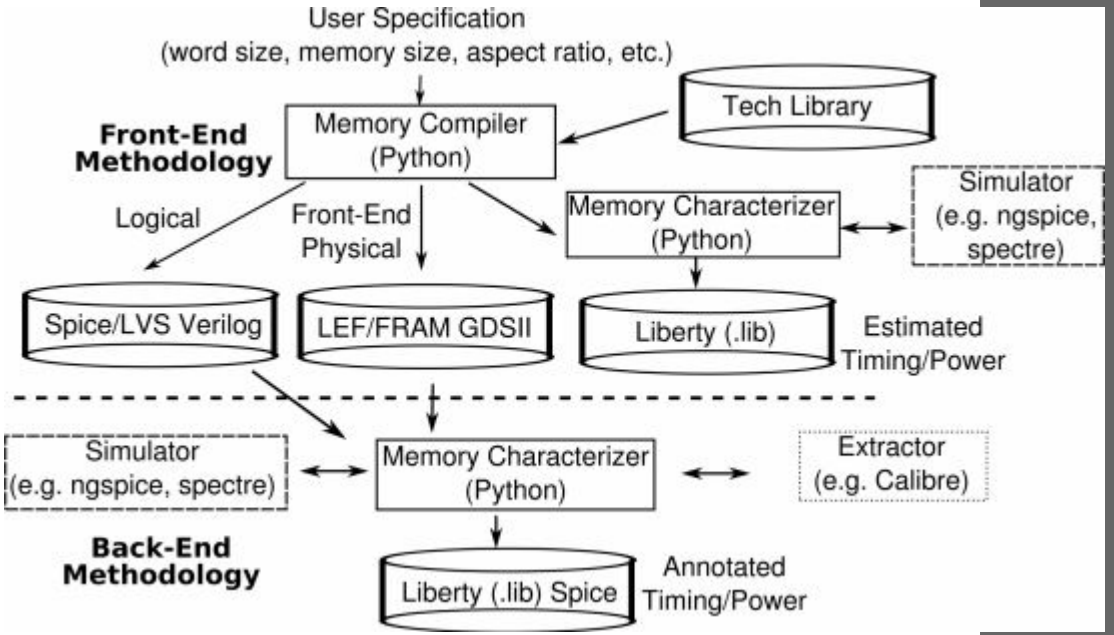
- Adding more access ports is expensive
  - Scaling from 1 to 2 ports doubles amount of wires
- Wires are often limiting factor
  - Leads to ~n^2 scaling for adding ports
- SRAMs with more ports are often less dense, harder to find





Ram Compilers

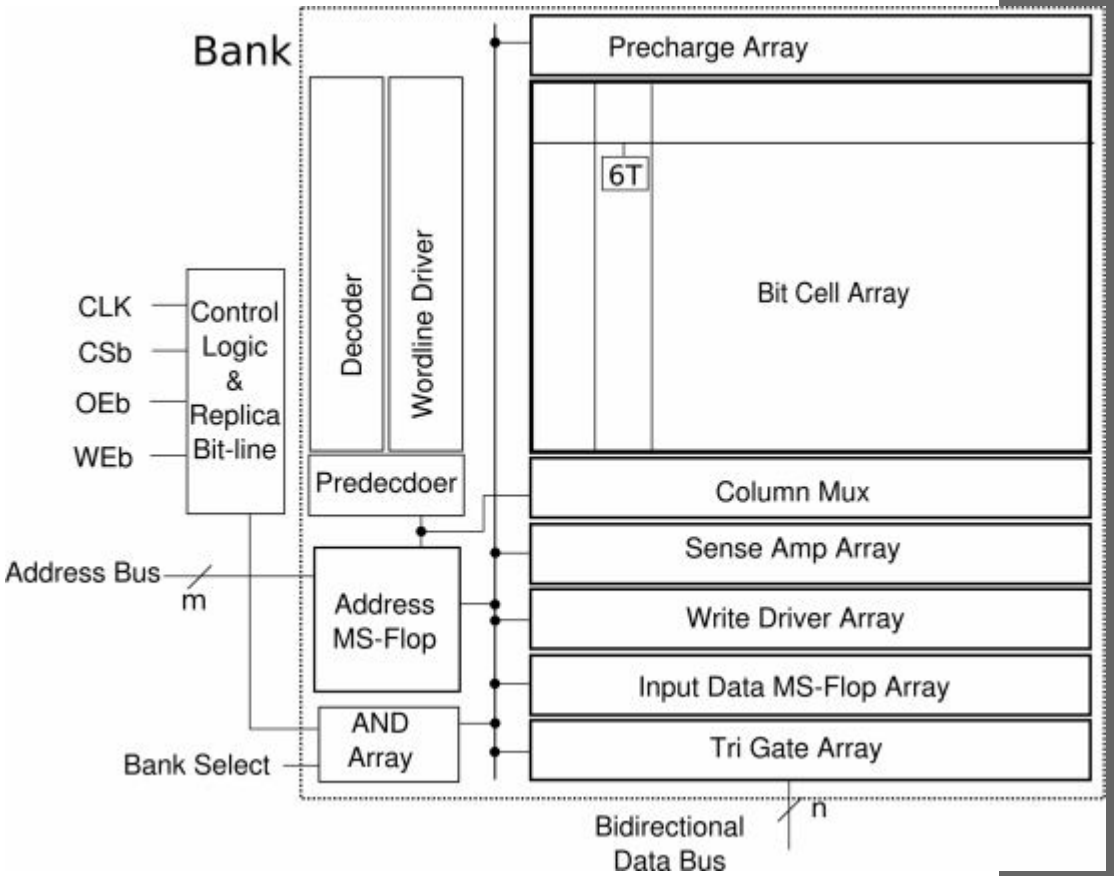
- How do we design RAM to fit our needs?
  - What if there is not pre-existing IP for our use case?
- Solution: Ram Compilers
  - RAM is made of repetitive structures
  - Copy analog structures automatically
- Characterizes RAM
  - Generates SPICE and simulates electrically
  - Creates timing file (.lib)
  - Creates verilog models



OpenRAM

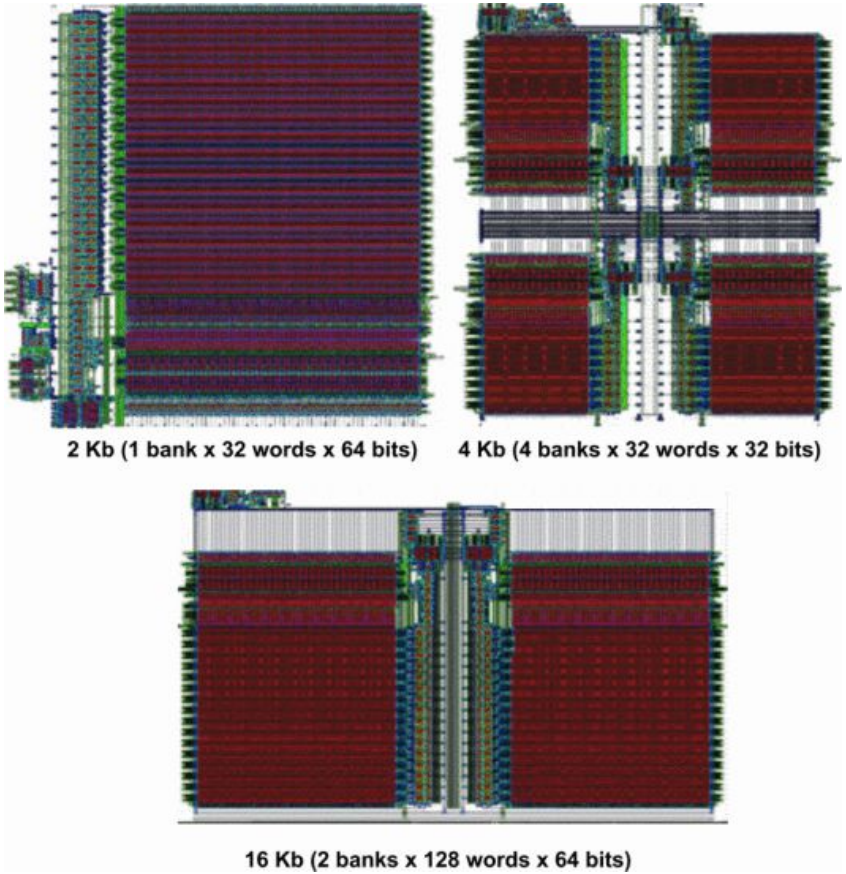
- Many RAM compilers are highly expensive
  - Good RAM is valuable IP
- OpenRAM → Open Source alternative

- Breaks RAM down into basic elements
  - Sense Amps to Read, Address Decoders, etc.
  - Not PDK specific



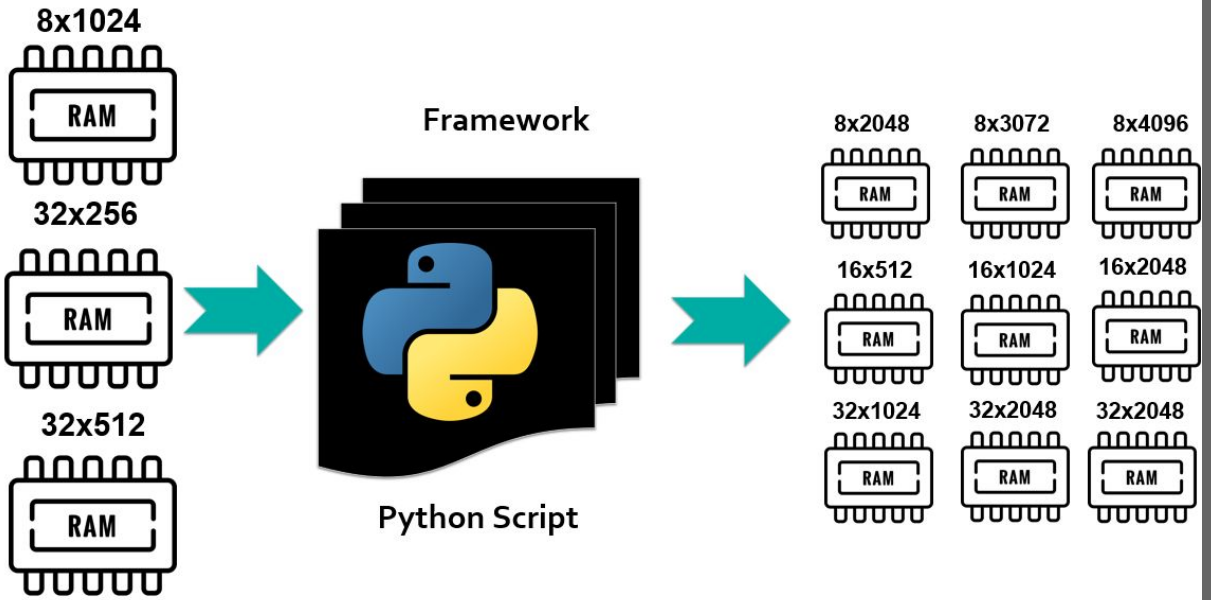
OpenRAM

- User/Community implements most basic modules
  - Each PDK needs its own implementation
- Compiler arranges and scales modules based on input sizes
  - Always a power of 2
- Outputs spice, gds, etc.



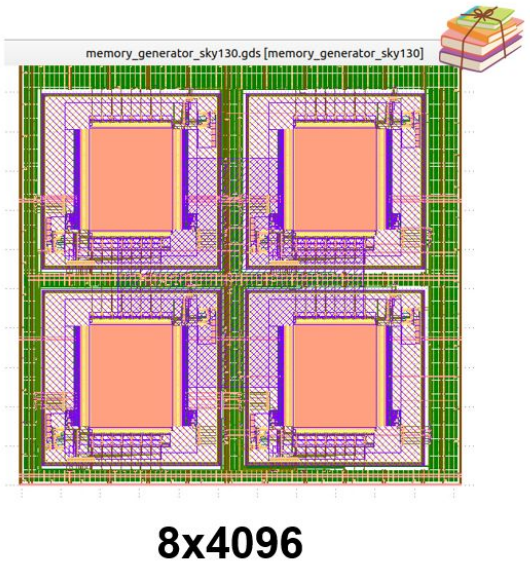
Ram Layout & Interleaving Tools

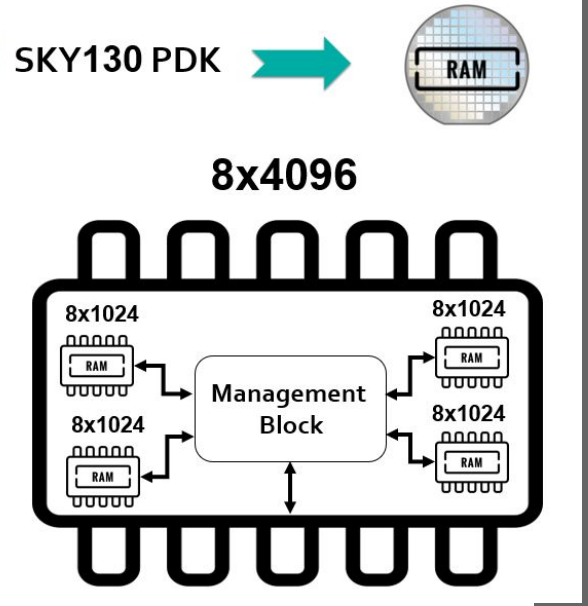
- Sometimes SRAM compilers are not enough
  - Almost always limited to powers of 2 for size and width
  - Compiling your own SRAM is difficult
- Solution: Combine existing IP into new sizes
  - Ram Layout tools help combine modules into new sizes



Ram Layout Tools

- Solution: Combine existing IP into new sizes
  - Ram Layout tools help combine modules into new sizes
- Tools create:
  - Interconnects between rams in verilog
  - Macro positions
- Can scale to non powers of 2



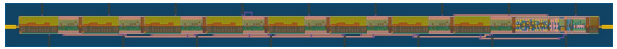


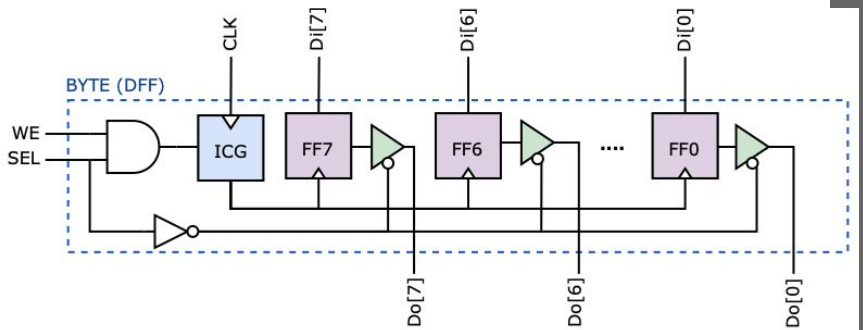
Glossary

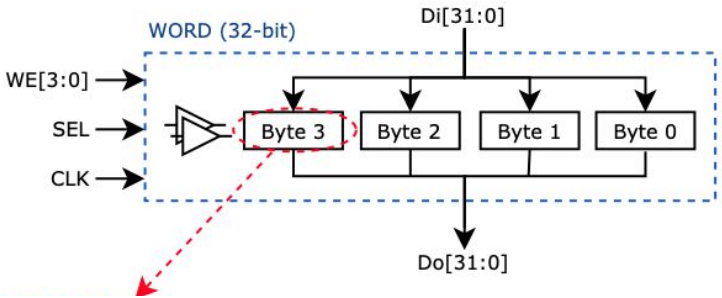
DFFRAM: D-Flip-Flop Ram

DFFRAM

- Problem 1: SRAM is hard to validate
  - Simulation is done with behavioral model, not actual hardware
- Problem 2: SRAM doesn't work on OpenLane2
  - Only works on OpenLane1
- Solution: DFFRAM
  - Array of Densely Packed Flip Flops
  - Purely digital (no analog elements)
  - Can do gate-level simulation of cells
- 20-30 Transistors per Bit
  - ~5x worse density than SRAM
  - ~5x better than declaring a 2d array in verilog

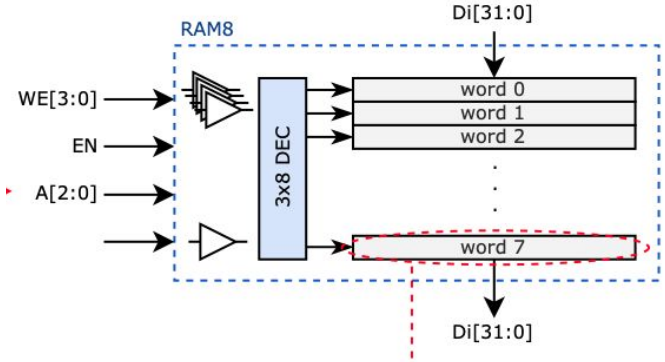




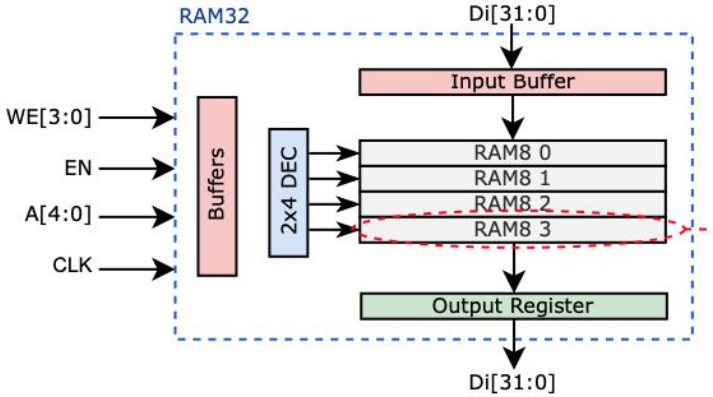


DFFRAM - Scaling Up

- Built using Recursive Macros
  - 8 DFFs make a byte, 4 bytes make a word
  - Words are stacked vertically to make rams
  - 8 Words Stacked makes a RAM8
  - 2 RAM8s make a RAM16, etc.



- Provides macros generally up 512 words (2 KB)
  - Most have 1 read/write port
  - Some have 2 ports but on the smaller end of capacity



Glossary

DRAM: Dynamic RAM
SDRAM: Synchronous DRAM
DDR: Double Data Rate

DRAM

- 1 Transistor per Bit
  - At least 6x denser than SRAM
- Highest Density Ram Available
  - Not usable on SKY130
  - Generally requires specific PDK
  - Often used off-chip
- Destructive Reads
  - Bits can only be read once
  - Have to re-write after each read
- Requires Refreshes
  - Bits last temporarily
  - Have to be refreshed every milliseconds

DDR RAM

Also DDR RAM

"I don't think the highest density ram would be very good at DDR"

SONOS Flash

- Non-Volatile Flash Memory On Chip!
  - Supported by SKY130!

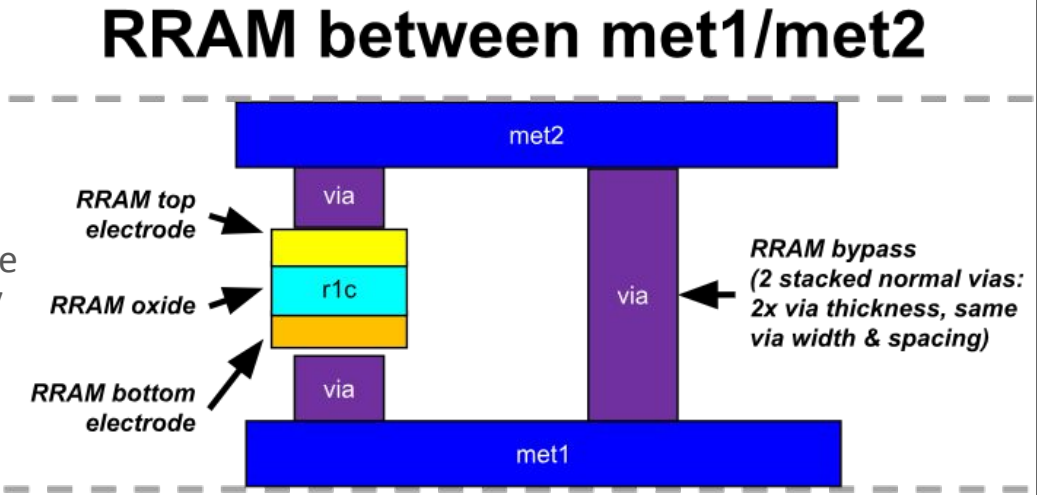
- Problem: requires fancy voltages to read and write
  - On the order of +10 and -3 volts
  - Usually digital chip only has +3.3 and +1.8 volts
  - Available as an analog cell
  - Yet to be wrapped in a usable macro

Glossary

RRAM: Resistive RAM

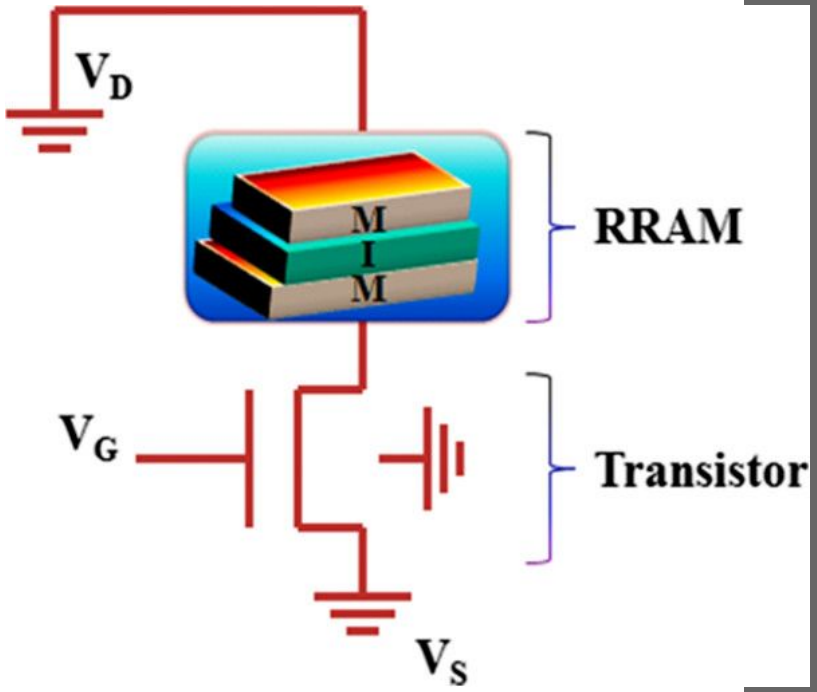
RRAM / ReRAM

- Store values in the resistance of a conductor
  - 1 -> Low Resistance
  - 0 -> High Resistance
- Use material that changes its resistance in an electric field
  - Resistance responds to voltage
  - Can be implemented vertically on chip
- Set/Reset using different voltages
- Read by Measuring Current
  - High Current ⟶ 1



RRAM Advantages

- Higher Density than SRAM
  - 1 transistor per bit
- Reads are efficient
  - Low latency
  - Low energy
- Non-Volatile
  - Holds resistive state on reset
  - Easier voltages than SONOS
- Can sometimes hold multiple bits per cell



RRAM Disadvantages

- Higher write latency than read latency
  - Writes involve physical structure change
- Limited endurance compared to volatile technologies (SRAM, DRAM)
  - Finite number of writes
- Misbehaves at very high temperatures
  - Changes resistance

Glossary

MRAM: Magnetoresistive RAM

MRAM

- Non Volatile, Similar to RRAM
  - Uses magnetic fields instead of electric fields to change resistance
  - Write by using the magnetic field of a current
- \+ Generally more reliable than RRAM
  - \+ More write cycles
  - \+ Not as sensitive to temperature
- \- More expensive and less dense than RRAM
- \- Sensitive to magnetic fields

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